AMENDMENTS TO THE CLAIMS

Claims 1 – 186. (cancel)

Claim 187. (new) A device, comprising:

a functional circuit, said functional circuit comprising:

a logic circuit; and

a variable delay; and

a latch;

wherein

said variable delay is coupled to receive input from a data path and coupled to provide output to the latch; and

said latch is coupled to receive input from the variable delay and provide input to said logic circuit; and

a control circuit, said control circuit comprising:

a register;

a repeater;

a comparator; and

a command detector;

wherein

said register is coupled to receive input from a first external source and coupled to provide output to said repeater and said comparator;

said repeater is coupled to receive input from said register and said command detector and to provide output to a second external source;

said command detector is coupled to receive input from said second external source and to provide output to said repeater and said comparator; and

said comparator is coupled to receive input from said latch of said functional circuit and said register and provide output to control said variable delay.

Claim 188. (new) The device of claim 187, wherein said first external source and said second external source are a same bus coupled to said device.

Claim 189. (new) The device of claim 188, wherein said device is a memory device and said logic circuit comprise a memory array.

Claim 190. (new) The device of claim 189, wherein said memory array comprises a plurality of dynamic random access memory (DRAM) cells.

Claim 191. (new) The device of claim 198, wherein said first external source is a register coupled to said device and said second external source is a bus coupled to said device.

Claim 192. (new) The device of claim 191, wherein said device is a memory controller and said logic circuit comprise a control logic for controlling a memory device.

Claim 193. (new) The device of claim 192, wherein said control logic is capable of operating a dynamic random access memory (DRAM) device.

Claim 194 (new) A system, comprising:

a bus;

a pattern register;

a first device, said first device coupled to said bus and said first device comprising:

a first functional circuit, said first functional circuit comprising:

a first logic circuit; and

a first variable delay; and

a first latch;

wherein

said first variable delay is coupled to receive input from a data path and coupled to provide output to the first latch; and

said first latch is coupled to receive input from the first variable delay and provide input to said first logic circuit; and

a first control circuit, said first control circuit comprising:

a first register;

a first repeater;

a first comparator; and

a first command detector;

wherein

said first register is coupled to receive input from said pattern register and coupled to provide output to said repeater and said first comparator;

said first repeater is coupled to receive input from said first register and said command detector and to provide output to said bus;

said first command detector is coupled to receive input from said bus and to provide output to said repeater and said first comparator; and

said first comparator is coupled to receive input from said latch of said first functional circuit and said first register and provide output to control said first variable delay; and

a second device, said second device coupled to the bus and said second device comprising:

a second functional circuit, said second functional circuit comprising:

a second logic circuit; and

a second variable delay; and

a second latch;

wherein

said second variable delay is coupled to receive input from the data path and coupled to provide output to the second latch; and

said second latch is coupled to receive input from the second variable delay and provide input to said second logic circuit; and

a second control circuit, said second control circuit comprising:

a second register;

a second repeater;

a second comparator; and

a second command detector;

wherein

said second register is coupled to receive input from said bus and coupled to provide output to said repeater and said second comparator;

said second repeater is coupled to receive input from said second register and said command detector and to provide output to said bus;

said second command detector is coupled to receive input from said bus and to provide output to said repeater and said second comparator; and

said second comparator is coupled to receive input from said latch of said second functional circuit and said second register and provide output to control said second variable delay.

Claim 195. (new) The system of claim 194, wherein said first device is a memory controller.

Claim 196. (new) The system of claim 194, wherein said second device is a memory device.